REMARKS

The Office Action dated September 30, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Applicants acknowledge that the previous Office Action of June 1, 2004, requiring a restriction in this application, has been vacated. Applicants wish to thank the Examiner for accepting the traversal of the restriction requirement. As a result, Claims 1-4 and 6-20 are currently pending in the application, and are respectfully submitted for consideration.

In the Office Action, claims 1-4 and 6-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over McAllister (U.S. Patent No. 6,501,755) in view of Hine (U.S. Patent No. 5,652,864). The Office Action took the position that McAllister discloses all of the elements of the claimed invention, with the exception of passing off the released memory address in place of the available memory address when the release of the released memory address occurs in the same clock cycle as the request for the available address. The Office Action then relies upon Hine to cure this deficiency in McAllister. The above rejection is respectfully traversed for the reasons which follow.

Claim 1, upon which claim 2 is dependent, recites a method for managing memory in a network switch. The method includes the steps of providing a memory including a plurality of memory locations configured to store data therein, providing a memory address pool having a plurality of available memory addresses arranged therein, wherein each of the plurality of memory addresses corresponds to a specific memory location, and

providing a memory address pointer, wherein the memory address pointer indicates a next available memory address in the memory address pool. When a release of a released memory address does not occur in a same clock cycle as a request for an available address, the method further includes reading available memory addresses from the memory address pool using a last in first out operation, writing released memory addresses into the memory address pool, and adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool. When the release of the released memory address occurs in the same clock cycle as the request for the available address, the method further includes passing off the released memory addresses in place of the available memory addresses.

Claim 3, upon which claim 4 is dependent, recites a method for managing memory in a network switch. The method includes the steps of receiving a request from a module for a next available memory address in a first clock cycle, and receiving a released memory address in the first clock cycle. The method also includes passing off the released memory address to the module requesting the next available memory address in place of the next available memory addresses in a second clock cycle, which is a next clock cycle after the first clock cycle.

Claim 6, upon which claim 7 is dependent, recites a method for managing memory. The method includes the steps of providing a memory having a predetermined number of memory storage locations therein, providing a predetermined number of addresses in a stack, each of the predetermined number of addresses corresponding to a

unique memory storage location, and providing an address pointer for indicating a next available address to be used from the predetermined number of addresses in the stack, wherein the address pointer releases an address in a last-in first-out type operation. The method further comprises a step of passing off an address released back to the stack to a request for an available address in place of a next available memory address when a release of an address back to the stack occurs in the same clock cycle as the request for an available address.

Claim 8, upon which claims 9-12 are dependent, recites an apparatus for managing memory in a network switch. The apparatus includes a memory address pool having a plurality of memory addresses, each of the plurality of memory addresses corresponding to an individual memory location in a memory. The apparatus also includes a memory controller in connection with the memory and the memory address pool. The memory controller manages an address pointer for indicating a next available memory address in the memory address pool and is configured to pass off the released memory address in place of the available memory address upon a request for the available memory address in the same clock cycle.

Claim 13, upon which claims 14-19 are dependent, recites an apparatus for managing memory in a network switch. The apparatus includes a memory address pool in connection with the memory, the memory address pool having a predetermined number of memory addresses therein, each of the predetermined number of memory addresses corresponding to an individual memory location in the memory. The apparatus

also includes a memory controller in connection with the memory and the memory address pool. The memory controller passes off a released memory address to a request for an available memory address in place of the available memory address when the request for the available memory address is received during the same clock cycle as the released memory address is released.

Claim 20 recites an apparatus for managing memory in a network switch. The apparatus includes a memory having a plurality of memory locations configured to store data therein, a memory address pool having a plurality of available memory addresses arranged therein, wherein each of the plurality of memory addresses corresponds to a specific memory location. The apparatus further includes means for managing a memory address pointer, wherein the memory address pointer indicates a next available memory address in the memory address pool, means for reading available memory addresses from the memory address pool using a last in first out operation, means for writing released memory addresses into the memory address pool, and means for adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool. The means for reading and the means for writing are configured to pass off an available memory address in place of a next available memory address when a request to read an address is received during the same clock cycle as a request to write an address.

As will be discussed below, McAllister and Hine fail to disclose or suggest all of the elements of the claims, and therefore fail to provide the features discussed above.

McAllister discloses stacked address transport in connection oriented networks. More specifically, McAllister discloses a method of signaling a message using a terminal across multiple network entities. At least two contiguous network entities are associated with addressing spaces for which message addresses are not routable by way of the terminal address and are not otherwise routable by way of a single address. The message is initiated from the terminal originating address associated with the originating network entity and is routed through the intermediate network entities to be received at the terminal destination address associated with the terminating network entity.

Hine discloses concurrent allocation requests in a computer system. Available storage blocks are chained together. A length of the respective block and a pointer to a next block in the chain are stored in each block. The chain is searched to identify one of the available blocks to satisfy one storage allocation request while permitting allocation of another block on the chain pursuant to another storage allocation request. While permitting allocation of another block on the chain, access to the one block is prevented pursuant to the other request.

With respect to the rejection of claim 1, Applicants respectfully submit that the combination of McAllister and Hine fails to disclose or suggest reading available memory addresses from the memory address pool using a last in first out operation, writing released memory addresses into the memory address pool, and adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool when a release of a released memory address does not occur in a same clock

cycle as a request for an available address, as recited in claim 1. Even if it were acknowledged by Applicants that McAllister discloses the steps of reading, writing and adjusting, as alleged in the Office Action, McAllister fails to disclose or suggest that these steps are to take place when the release of a released memory address does not occur in the same clock as a request for an available address. McAllister only discloses that a party number is pushed onto a message stack, a replacement address for the party number is read by a processor, and determining whether the party number is to be discarded or replaced (McAllister, Column 19, lines 20-47). McAllister, however, makes no mention of the release of a released memory address not occurring in the same clock cycle as a request for an available address. Hine also fails to disclose such a limitation.

Additionally, Applicants respectfully submit that the combination of McAllister and Hine fails to disclose or suggest passing off the release memory address in place of the available memory address when the release of the released memory address occurs in the same clock cycle as the request for the available address, as recited in claims 1, 6, 8, 13, and 20. The Office Action acknowledges that McAllister fails to disclose such a limitation and relies on Hine as disclosing this element of the claims. Applicants respectfully submit that Hine also fails to disclose or suggest such a limitation. Hine, as mentioned above, discloses searching a chain to identify an available block to satisfy one storage allocation request while permitting allocation of another block on the chain pursuant to another storage allocation request (Hine, Column 7, line 30 – Column 8, line 34). Hine, however, does not teach or suggest that the passing off occurs when the

release of the released memory address occurs in the same clock cycle as the request for the available address. Both McAllister and Hine fail to disclose this limitation of the claims. Thus, the combination of McAllister and Hine fail to disclose or suggest all of the elements of claims 1, 6, 8, 13, and 20.

Applicants note that claims 2, 7, 9-12, and 14-19 are dependent upon claims 1, 6, 8, and 13, respectively. Therefore, Applicants submit that claims 2, 7, 9-12, and 14-19 should be found allowable for at least their dependence upon claims 1, 6, 8, and 13, and for the specific limitations recited therein.

With respect to the rejection of claim 3, Applicants respectfully submit that the combination of McAllister and Hine fail to disclose or suggest "passing off the released memory address to the module requesting the next available memory address in place of the next available memory addresses in a second clock cycle, which is a next clock cycle after the first clock cycle," as recited in claim 3. The Office Action acknowledges that McAllister fails to disclose this limitation of the claim, and relies on Hine as teaching this element of the claim. Applicants respectfully assert that Hine also fails to disclose such a limitation. Hine, as stated above, discloses searching a chain to identify an available block to satisfy one storage allocation request while permitting allocation of another block on the chain pursuant to another storage allocation request (Hine, Column 7, line 30 – Column 8, line 34). Hine, however, fails to disclose passing off the released memory address to the module requesting the next available memory address in place of the next available memory addresses in a second clock cycle. McAllister, as

acknowledged in the Office Action, also fails to disclose such a limitation. Therefore, McAllister and Hine, whether viewed singly or in combination, fail to disclose or suggest all of the elements of claim 3.

Claim 4 is dependent upon claim 3 and should be found allowable for at least its dependence upon claim 3, and for the specific limitations recited therein.

Applicants respectfully submit that McAllister and Hine, whether viewed alone or in combination, fail to disclose or suggest critical and important elements of the claimed invention. These distinctions are more than sufficient to render the claimed invention unanticipated and unobvious. It is therefore respectfully requested that all of claims 1-4 and 6-20 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

Majid S. AlBassam
Registration No. 54,749

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

MSA:jf